H-721-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application: Y. ITOU et al
USSN 09/266,634
Filed: March 11, 1999

Group Art Unit: 2122
Examiner: C. Das
For: METHOD OF REDUCING UNNECESSARY BARRIER INSTRUCTIONS

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE SPECIFICATION

Please amend the specification as set forth below.

Page 1, before the first line of the specification please insert the sentence:

--This application is a continuation application of U.S. Serial No. 09/266,634, filed March 11, 1999.--

IN THE CLAIMS

Cancel claim 1, and add claims 18-20 as follows.

--18. A method of reducing unnecessary barrier instructions in a compiler for generating a parallel processing object program from a source program, comprising:

transforming with said compiler said source program into parallel processing execution divisions,

deleting a barrier instruction when between parallel processing execution divisions, no dependency exists between a variable or array reference to be referenced and a following reference.

--19. A method of reducing unnecessary barrier instructions in a compiler for generating a parallel processing object program from a source program, comprising:

transforming with said compiler said source program into parallel processing execution divisions,

deleting a barrier instruction when between parallel processing execution divisions, a dependency exists between a variable or array reference to be referenced and a following reference, and this dependency is only within the same parallel processing execution division and no dependency exists between different parallel processing execution divisions.

--20. A method of reducing unnecessary barrier instructions in a compiler for generating a parallel processing object program from a source program, comprising:

transforming with said compiler said source program into parallel processing execution divisions,

deleting a barrier instruction when memory coherence processing has been completed at a memory location at which a dependent relation occurs between parallel processing execution divisions.--

REMARKS

Examination is respectfully requested.

Respectfully submitted,

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